SN74ALVCHG162280 16-BIT TO 32-BIT REGISTERED BUS EXCHANGER WITH BYTE MASKS AND 3-STATE OUTPUTS

SCES093D-FEBRUARY 1997-REVISED OCTOBER 2004

FEATURES

- Member of the Texas Instruments Widebus™
 Family
- EPIC[™] (Enhanced-Performance Implanted CMOS) Sub-Micron Process
- A-Port Outputs Have Equivalent 50- Ω Series Resistors and B-Port Outputs Have Equivalent 20- Ω Series Resistors, So No External Resistors Are Required
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Packaged in Thin Very Small-Outline Package

NOTE: For order entry, the DBB package is abbreviated to G. For tape and reel, the DBBR package is abbreviated to GR.

DESCRIPTION

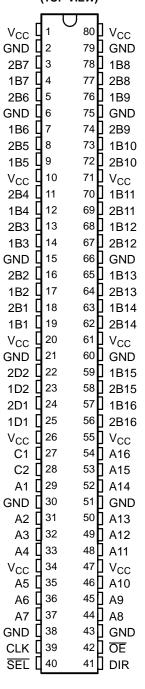
The SN74ALVCHG162280 is a 16-bit to 32-bit registered bus exchanger. This device is intended for use in applications where data must be transferred from a narrow high-speed bus to a wide lower-frequency bus. It is designed specifically for low-voltage (3.3-V) $V_{\rm CC}$ operation.

The device provides synchronous data exchange between the two ports, A and B. Data is stored in the internal registers on the low-to-high transition of the clock (CLK) input. For data transfer in the B-to-A direction, the select (SEL) input selects 1B or 2B data for the A outputs.

For data transfer in the A-to-B direction, a two-stage pipeline is provided in the 1B path, with a single storage register in the 2B path. Data flow is controlled by the active-low output-enable (\overline{OE}) and direction-control (DIR) inputs. DIR is registered to synchronize the bus direction changes with the clock.

Two mask bits are provided for both data bytes. The data (D) outputs are controlled by $\overline{\text{OE}}$.

DBB PACKAGE (TOP VIEW)





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DESCRIPTION (CONTINUED)

The A-port N-channel output transistors are sized at 450 μ m, and the P-channel output transistors are sized at 700 μ m. All A-port outputs have equivalent 50- Ω series resistors. The B-port N-channel output transistors are sized at 225 μ m, and the P-channel output transistors are sized at 560 μ m. All B-port outputs have equivalent 20- Ω series resistors.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The switching characteristics are based on 25-pF (A port) and 80-pF (B and D ports) loads, but are tested with the standard 50-pF load.

The SN74ALVCHG162280 is characterized for operation from 0°C to 70°C.



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FUNCTION TABLES

A-TO-B STORAGE (OE = L, DIR = H)

	INPUTS	OUTI	PUTS	
SEL	CLK	1B	2B 2B ₀ ⁽¹⁾ L	
Н	Х	Х	1B ₀ ⁽¹⁾	2B ₀ ⁽¹⁾
L	\uparrow	L	L ⁽²⁾	L
L	\uparrow	Н	H ⁽²⁾	Н

- Output level before indicated steady-state input conditions were established
- (2) Two CLK edges are needed to propagate the data.

B-TO-A STORAGE (OE = L, DIR = L)

	INP	JTS		OUTPUT
CLK	SEL	1B	2B	Α
1	Н	Х	L	L(1)
1	Н	Χ	Н	H ⁽¹⁾
1	L	L	Χ	L
1	L	Н	Χ	Н

(1) Two CLK edges are needed to propagate the data. The data is loaded in the first register when SEL is low and propagates to the second register when SEL is high.

C-TO-D STORAGE (OE = L)

	INPUTS	OUTPUTS			
SEL	CLK	С	1D	2D	
Н	Х	Х	1D ₀ ⁽¹⁾	2D ₀ ⁽¹⁾	
L	\uparrow	L	L ⁽²⁾	L	
L	\uparrow	Н	H ⁽²⁾	Н	

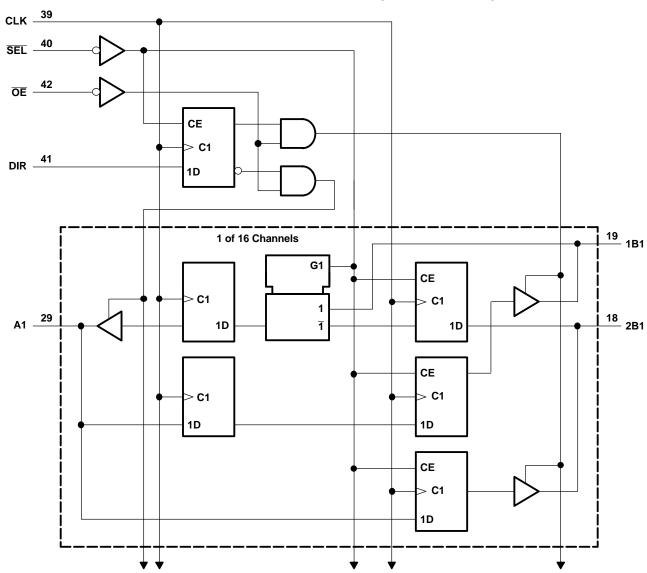
- Output level before indicated steady-state input conditions were established
- (2) Two CLK edges are needed to propagate the data.

OUTPUT ENABLE

	INPUTS			OUTPUTS	
CLK	ŌĒ	DIR	Α	1B, 2B	1D, 2D
1	Н	Х	Z	Z	Z
\uparrow	L	Н	Z	Active	Active
\uparrow	L	L	Active	Z	Active



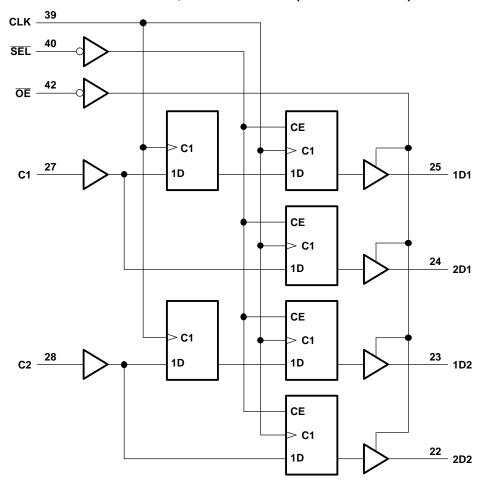
LOGIC DIAGRAM, A AND B PORTS (POSITIVE LOGIC)





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LOGIC DIAGRAM, C AND D PORTS (POSITIVE LOGIC)



ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{CC}	Supply voltage range		-0.5	4.6	V
V	Innut voltage range	Except I/O ports ⁽²⁾	-0.5	V _{CC} + 0.5	\/
V _I	Input voltage range	I/O ports ⁽²⁾⁽³⁾	-0.5	V _{CC} + 0.5	V
Vo	Output voltage range ⁽²⁾⁽³⁾		-0.5	V _{CC} + 0.5	V
I _{OK}	Output clamp current	V _O < 0		-50	mA
Io	Continuous output current			±50	mA
θ_{JA}	Package thermal impedance ⁽⁴⁾			106	°C/W
T _{stg}	Storage temperature rang	e	-65	150	°C

⁽¹⁾ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

⁽²⁾ The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

³⁾ This value is limited to 4.6 V maximum.

⁽⁴⁾ The package thermal impedance is calculated in accordance with JESD 51.

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RECOMMENDED OPERATING CONDITIONS⁽¹⁾

				MIN	MAX	UNIT
V _{CC}	Supply voltage	3	3.6	V		
V_{IH}	High-level input voltage $V_{CC} = 3 \text{ V to } 3.6 \text{ V}$					V
V_{IL}	Low-level input voltage $V_{CC} = 3 \text{ V to } 3.6 \text{ V}$				8.0	V
V_{I}	Input voltage	0	V_{CC}	V		
Vo	Output voltage				V_{CC}	V
1	High-level output current	A to B	V _{CC} = 3 V		8	mA
I _{OH}	riigii-ievei output current	B to A	$V_{CC} = 3 V$		6	IIIA
	Low-level output current	A to B	$V_{CC} = 3 V$		8	mA
IOL	Low-level output current	V _{CC} = 3 V		6	ША	
$\Delta t/\Delta v$	Input transition rise or fall rate				10	ns/V
T _A	Operating free-air temperature			0	70	°C

⁽¹⁾ All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

Р	ARAMETER	TEST CONDITIONS	V _{cc}	MIN	TYP ⁽¹⁾	MAX	UNIT
		I _{OH} = -100 μA	3 V to 3.6 V	V _{CC} - 0.2			
V_{OH}	A to B	I _{OH} = -8 mA	3 V	2			V
	B to A	I _{OH} = -6 mA	3 V	2			
		I _{OL} = 100 μA	3 V to 3.6 V			0.2	
V_{OL}	A to B	I _{OL} = 8 mA	3 V			0.8	V
	B to A	I _{OL} = 6 mA	3 V			0.8	
II		$V_I = V_{CC}$ or GND	3.6 V			±5	μΑ
		V _I = 0.8 V	3 V	75			
I _{I(hold)}		V _I = 2 V	3 V	-75			μΑ
		V _I = 0 to 3.6 V ⁽²⁾	3.6 V			±500	
I _{OZ} (3)		$V_O = V_{CC}$ or GND	3.6 V			±10	μΑ
Icc		$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V			40	μΑ
ΔI_{CC}		One input at V_{CC} - 0.6 V, Other inputs at V_{CC} or GND	3 V to 3.6 V			750	μΑ
^	Control inputs	V V T OND	0.01/		4		
Ci	C port	$V_{I} = V_{CC}$ or GND	3.3 V		8.5		pF
Co	D port	$V_O = V_{CC}$ or GND	3.3 V		7		pF
Cio	A or B ports	$V_O = V_{CC}$ or GND	3.3 V		8.5		pF

⁽¹⁾ All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

⁽²⁾ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

⁽³⁾ For I/O ports, the parameter I_{OZ} includes the input leakage current.



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TIMING REQUIREMENTS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

			V _{CC} = ± 0.3	3.3 V 3 V	UNIT
			MIN	MAX	
f _{clock}	Clock frequency			160	MHz
t _w	Pulse duration, CLK high or low		2.3		ns
		A data before CLK↑	1.4		
		B data before CLK↑	2		
t_{su}	Setup time, high or low	C data before CLK↑	1.3		ns
		DIR before CLK↑	2		
		SEL before CLK↑	2		
		A data after CLK↑	0.3		
		B data after CLK↑	0.3		
t _h	Hold time, high or low	C data after CLK↑	0.3		ns
		DIR after CLK↑	0.3		
		SEL after CLK↑	0.3		

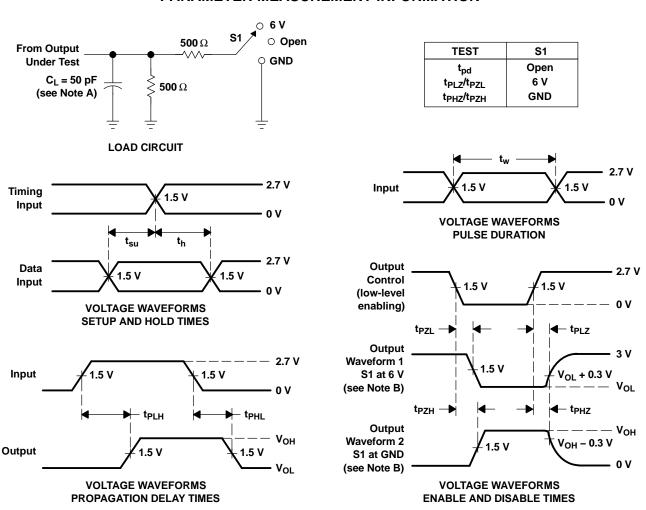
SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $C_L = 25 \text{ pF}$ (A port), 80 pF (B and D ports) (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	TO	V _{CC} = ± 0.3	UNIT	
	(INPUT)	(OUTPUT)	MIN	MAX	
f _{max}			160		MHz
		A	1.5	5	
t _{pd}	CLK	В	1.5	7.4	ns
		D	1.5	7.2	
	CLK	A	1.5	6.2	
	CLK	В	1.5	9.4	
t _{en}		A	1.5	6	ns
	ŌĒ	В	1.5	9.5	
		D	1.5	7.9	ns
	CLK	A	1.5	6.4	
	CLK	В	1.5	7.8	
t _{dis}		A	1.5	5	ns
	ŌĒ	В	1.5	7.6	
		D	1.5	6.7	



PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , $t_r \leq$ 2.5 ns. $t_f \leq$ 2.5 ns.
 - D. The output is measured with one input transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en}.
 - G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms





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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
74ALVCHG162280GRE4	ACTIVE	TSSOP	DBB	80	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ALVCHG162280GRG4	ACTIVE	TSSOP	DBB	80	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVCHG162280DBBR	OBSOLETE	TSSOP	DBB	80		TBD	Call TI	Call TI
SN74ALVCHG162280GR	ACTIVE	TSSOP	DBB	80	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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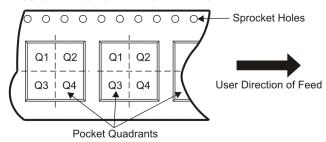
TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

	Device		Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SI	N74ALVCHG162280GR	TSSOP	DBB	80	2000	330.0	24.4	8.4	17.3	1.7	12.0	24.0	Q1





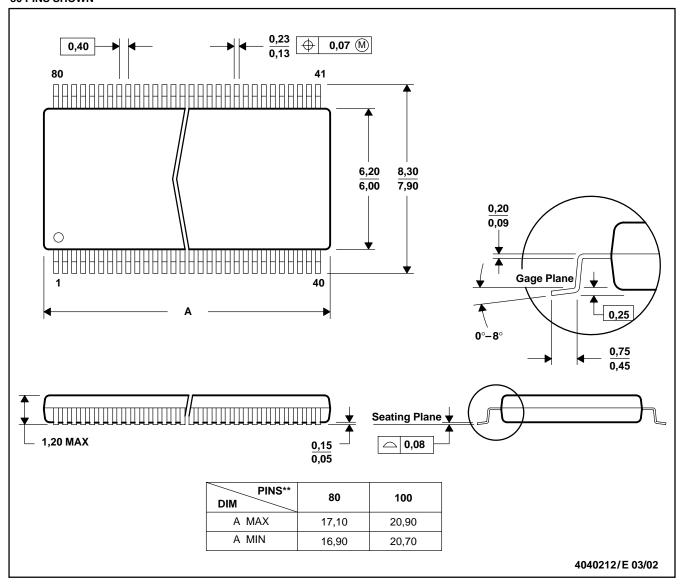
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALVCHG162280GR	TSSOP	DBB	80	2000	346.0	346.0	41.0

DBB (R-PDSO-G**)

80 PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Falls within JEDEC: 80 Pin - MO-153 Variation FF

100 Pin - MO-194 Variation BB

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